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<p>(54) Title: TRENCH-GATE SEMICONDUCTOR DEVICES AND THEIR MANUFACTURE</p> <p>(57) Abstract</p> <p>In a trench-gate semiconductor device, for example a cellular power MOSFET, the gate (11) is present in a trench (20) that extends through the channel-accommodating region (15) of the device. An underlying body portion (16) that carries a high voltage in an off state of the device is present adjacent to a side wall of a lower part (20b) of the trench (20). Instead of being a single high-resistivity region, this body portion (16) comprises first regions (61) of a first conductivity type interposed with second regions (62) of the opposite second conductivity type. In the conducting state of the device, the first regions (61) provide parallel current paths through the thick body portion (16), from the conduction channel (12) in the channel-accommodating region (15). In an off-state of the device, the body portion (16) carries a depletion layer (50). The first region (61) of this body portion (16) is present between the second region (62) and the side wall (22) of the lower part (20b) of the trench (20) and has a doping concentration (Nd) of the first conductivity type that is higher than the doping concentration (Na) of the second conductivity type of the second region (62). A balanced space charge is nonetheless obtained by depletion of the first and second regions (61, 62), because the width (W1) of the first region (61) is made smaller than the width (W2) of the lower-doped second region (62). This device structure can have a low on-resistance and high breakdown voltage, while also permitting its commercial manufacture using dopant out-diffusion from the lower trench part (20b) into the lower-doped second region (62) to form the first region (61).</p>		

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DESCRIPTION

**TRENCH-GATE SEMICONDUCTOR DEVICES AND THEIR
MANUFACTURE**

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This invention relates to trench-gate semiconductor devices, and particularly but not exclusively to trench-gate power MOSFETs which are insulated-gate field-effect devices. The invention also relates to methods of manufacturing such devices.

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Trench-gate semiconductor devices are known, comprising a semiconductor body including a channel-accommodating region of a second conductivity type between source and drain regions of an opposite first conductivity type. The source region is adjacent a major surface of the body, from which surface a trench extends through the channel-accommodating region and into an underlying body portion between the channel-accommodating region and the drain region. A gate is present in the trench and capacitively coupled to the channel-accommodating region adjacent to a side wall of the trench between the gate.

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An advantageous trench-gate semiconductor device is described in the ISPSD'98 paper "Simulated Superior Performances of Semiconductor Superjunction Devices" by T. Fujihira and Y. Miyasaka, pages 423 to 426 of the Proceedings of 1998 International Symposium on Power Semiconductor Devices & ICs, Kyoto. In this ISPSD'98 device the body portion comprises first regions of the first conductivity type interposed with second regions of the second conductivity type. This ISPSD'98 device is a particular embodiment of the advantageous general device type that was disclosed in United States patent specification US-A-4,754,310 (our ref. PHB32740). The interposed first and second regions serve to carry a depletion layer from the drain region to the channel-accommodating region in an off state of the device and to provide parallel current paths along the first regions in a conducting state of the device. A significant improvement is obtained in the relationship between the on-

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resistance and breakdown voltage of the device, by providing these interposed regions instead of a single high-resistivity body portion as conventionally used. The whole contents of both the ISPSD'98 paper and US-A-4,754,310 are hereby incorporated herein as reference material.

5 Published German patent application DE-A-197 36 981 describes the manufacture of other particular trench-gate device embodiments of this advantageous device type having interposed first and second regions. The whole contents of DE-A-197 36 981 are also hereby incorporated herein as reference material. In the manufacturing processes disclosed in DE-A-
10 197 36 981, deep trenches are formed in the semiconductor body, to the depth of the drain region. Both the first and second regions are diffused regions formed at the lower part of the deep trenches by ion-implanting dopants of opposite conductivity types at opposite facing sidewalls of neighbouring trenches and then diffusing the implanted opposite-conductivity-type dopants
15 until they meet to form a p-n junction in the intermediate body portion between the opposite facing sidewalls of the neighbouring trenches. The gate is formed in an upper part of the trench, capacitively coupled to the channel-accommodating region adjacent to a side wall of this upper part.

 In practice, the device structures and processes disclosed in
20 DE-A-197 36 981 can be difficult to implement in a volume-manufacturing and commercial context. It is difficult to ion implant dopants at the side walls of the lower part of narrow deep trenches, and so wider trenches than required for the trench-gate itself may be used. Furthermore some of the processes disclosed in DE-A-197 36 981 provide dielectric-filled trenches underneath the
25 source, which may have an undesired effect in increasing the device cell area between neighbouring channels and hence increasing the on-resistance of the device.

 It is an aim of the present invention to provide a trench-gate
30 semiconductor device which is of the advantageous device type that comprises interposed first and second regions and which has a device structure that is particularly appropriate for obtaining a low on-resistance while

permitting its manufacture using processes appropriate in a commercial volume-manufacturing context.

According to the present invention, there is provided a trench-gate semiconductor device having the features set out in Claim 1.

5 In trench-gate devices in accordance with the present invention, there are upper and lower parts to the trench. The trench-gate is present in an upper part, with the channel-accommodating region adjacent thereto. The relationship between on-resistance and breakdown-voltage of the device is improved by including the interposed first and second regions between the
10 drain region and the channel-accommodating region, adjacent to a lower part of the trench. The first regions provide parallel current paths between the conduction channel and the drain region, and they are present between the second region and the side wall of the lower part of the trench. The doping concentration of the first conductivity type of the first region is higher than the
15 doping concentration of the second conductivity type of the second region, so further reducing the on-resistance. However the charge of the space-charge region in the depleted body portion can still be adequately balanced because the width of the first region (measured perpendicular to the side wall of the trench) is made smaller than the width of the second region.

20 Such a construction is particularly appropriate for accommodating the first and second regions in a commercial trench-gate context, and it permits the device to have a low on-resistance due to the high doping concentration of the first regions that provide the parallel current paths between the conduction channel and the drain region. The high doping concentration of the narrow
25 first region may typically correspond to a dopant diffusion profile from the lower part of the trench into a body portion that provides the second region. This device construction is convenient for commercial manufacture.

Thus, in accordance with another aspect of the invention, there is provided a method of manufacturing a trench-gate device wherein, into a body
30 portion of the second conductivity type, dopant of the first conductivity type is out-diffused from the trench, through at least a side wall of a lower part of a trench so as to form the first region. The doping concentration of the second

region is provided by the body portion of the second conductivity type, which may be typically an epitaxial layer having, for example, a uniform doping concentration of the second conductivity type. The diffused dopant of the first conductivity type (out-diffused from, for example, a doped layer in the trench) provides the first region with a doping concentration of the first conductivity type that is higher than the doping concentration of the second conductivity type of the body portion. Its diffusion depth (measured perpendicular to the side wall of the trench) is less than the remaining width of the body portion (measured perpendicular to said side wall) that provides the second region.

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These and other features in accordance with the present invention are illustrated in embodiments of the invention which are now to be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a diagrammatic cross-sectional view of an active central part of a cellular trench-gate semiconductor device in accordance with the invention;

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Figure 2 is a simplified cross-sectional representation of half a cell of the device of Figure 1, from the centre of one cell to the centre of the adjacent trench-gate;

Figure 3 is a similar representation to Figure 2, but at a stage in the manufacture of the device using a method in accordance with the present invention;

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Figure 4 is a graph of simulated device characteristics of breakdown voltage V_B in volts and on-resistance R_{on} in ohm.mm^2 , for a specific example of the device of Figures 1 and 2 (point A) and for a conventional device (point B);

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Figure 5 is a similar simplified cross-sectional representation to Figure 2, of half a cell of a modification of the device that is also in accordance with the present invention; and

Figure 6 is a diagrammatic cross-sectional view of an active central part of a variant cellular trench-gate semiconductor device, also in accordance with the invention.

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It should be noted that Figures 1, 2, 3, 5 and 6 are diagrammatic, and their relative dimensions and proportions of parts of the drawings have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings. The same reference signs are generally used to refer to
5 corresponding or similar features in modified and different embodiments.

Figure 1 illustrates an exemplary embodiment of a trench-gate semiconductor device in the form of a cellular power MOSFET, comprising transistor cell areas 1 in a semiconductor body 10. Typically the device body 10
10 is of monocrystalline silicon. Each cell area 1 comprises a channel-accommodating region 15 of a second conductivity type (i.e. p-type in this example) between source and drain regions 13 and 14, respectively, of an opposite first conductivity type (n-type in this example). From a top major surface 10a of the body, a trench 20 extends through the
15 channel-accommodating region 15 and into an underlying body portion 16 between the channel-accommodating region 15 and the drain region 14. The trench-gate 11 is present in an upper part 20a of the trench 20 and is capacitively coupled to the channel-accommodating region 15 adjacent to a side wall 21 of the upper part 20a of the trench 20. The application of a voltage
20 signal to the gate 11 in a conducting state of the device serves in known manner for inducing a conduction channel 12 (of electrons in this example) in the region portion 15a and for controlling current flow in this conduction channel 12 between the source and drain regions 13 and 14. The source region 13 is located adjacent to the top major surface 10a of the device body, where it is contacted by
25 a source electrode 33. By way of example, Figure 1 shows a MOSFET device structure in which the drain region 14 is a substrate region of high conductivity adjacent to the opposite major surface 10b, where it is contacted by a drain electrode 34.

This MOSFET is of the advantageous general device type described in
30 US-A-4,754,310, the ISPSD'98 paper and DE-A-197 36 981. Thus, the thick body portion 16 that carries a high voltage in an off-state of the device is not a single high-resistivity region. Instead, the body portion 16 comprises first

regions 61 of the first conductivity type interposed with second regions 62 of the second conductivity type. In the conducting state of the device, the first regions 61 provide parallel current paths through the thick body portion 16, from the conduction channel 12 as illustrated in Figure 1. In an off-state of the device, the thick body portion 16 carries a depletion layer 50 from the drain region 14 to the channel-accommodating region 15, for example as illustrated in broken outline in Figure 2. The regions 61 and 62 each have a dopant content of their respective conductivity type that produces a balanced space charge in the body portion 16 when depleted in this off-state.

10 This voltage-sustaining body portion 16 is adjacent to a lower part 20b of the trench 20, i.e. the trench 20 extends much deeper in the body 10 than the channel-accommodating region 15. In accordance with the present invention, the first region 61 of this body portion 16 is present between the second region 62 and the side wall 22 of the lower part 20b of the trench 20. In fact, the lower part 20b of the trench 20 carries the first region 61 through the body portion 16 to the drain region 14. This first region 61 has a doping concentration N_d of the first conductivity type that is higher than the doping concentration N_a of the second conductivity type of the second region 62. A balanced space charge is nonetheless obtained between the regions 61 and 62, because the width W_1 (measured perpendicular to the side wall 22) of this higher-doped first region 61 is appropriately less than the width W_2 of the lower-doped second region 62.

The lower part 20b of the trench 20 is adapted to interface with the adjacent body portion 16 comprising its interposed first and second regions 61 and 62. Thus, its dimensions and composition are chosen in accordance with the desired voltage handing characteristics of the device. The depth of the lower part 20b of the trench 20 is determined in accordance with the desired thickness of the body portion 16, so as to accommodate the spread of the depletion layer 50 between the drain region 14 and the channel-accommodating region 15. The depth of the upper part 20a of the trench 20 is determined in accordance with desired channel length, and hence the length

of the trench-gate 11 in this upper part 20a, as well as the thickness of the channel-accommodating region adjacent thereto.

Typically, for devices designed to have moderate or high breakdown voltages, the depth of the lower part 20b of the trench 20 is larger, for example
5 an order of magnitude larger, than the depth of the upper part 20a of the trench 20. Thus, the first region 61 typically has a length L6 that is longer, for example an order of magnitude longer, than the length L5 of the channel-accommodating region 15. These lengths L5 and L6 are measured in the depth direction of the trench 20, and adjacent to the respective upper and
10 lower parts 20a and 20b of the trench 20. Thus, for example, the length L5 may be a few micrometres or less, whereas the length L6 may be more than 10 μm (micrometres), and even for example more than 20 μm or 30 μm or even 40 μm .

As illustrated in Figure 2, the first region 61 (adjacent to the lower part
15 20b of the trench 20) may be spaced from the channel-accommodating region 15 by a part 63 of the second region 62. This part 63 extends adjacent to the upper part 20a of the trench 20 where the trench-gate 11 is present. The gate 11 serves to induce an extension of the conduction channel 12 in this part 63 of the body portion 16. The inclusion of this low-doped part 63 serves to
20 relieve the field between the facing edges of the moderately highly doped regions 15 and 61. The length L3 of this part 63 may be, for example, a few micrometres or less.

Typically, the lower part 20b of the trench 20 comprises a material 17
having of a dielectric nature at least adjacent the side wall 22 of the lower part
25 20b of the trench 20. This dielectric material 17 may be an insulating material, for example silicon dioxide, or it may be an undoped (intrinsic) semiconductor material or a low-doped semiconductor material of the second conductivity type (p-type in this example). Thus, the lower part 20b of the trench 20 may be filled with an insulating material 17, or it may comprise, for example, a
30 semiconductor region 17 of the second conductivity type. This semiconductor region 17 may form a p-n junction with the adjacent first region 61 and is typically isolated from the gate 11 by an extension 24' of the gate insulating layer

24. However, the lower trench part 20b may comprise a low-doped semiconductor region 17' which is of the same conductivity type (n-type) as the side-wall adjacent region 61 and which is isolated from the gate 11. This low-doped n-type region 17' may adjoin the n-type region 61 and may fill the lower trench part 20b, or it may be separated from the n-type region 61 by a p-type region 17. The very low doping of such semiconductor regions 17 and 17' are such as to give an adequately balanced charge state in the space-charge region (when depleted together with the regions 61 and 62 in the voltage-sustaining off-state of the device), i.e. such that an electric field resulting from any imbalance is less than the critical field at which breakdown would occur in the semiconductor material.

The moderately high doping concentration of the narrow first region 61 typically corresponds to a dopant diffusion profile from the lower part 20a of the trench 20.

Thus, the device of Figure 1 is manufactured by a method which includes the steps of:

- etching a deep trench 20 into a body portion 60 (see Figure 3) of the second conductivity type (p-type in this example) having a doping concentration N_a for providing the second region 62, and
- out-diffusing dopant of the first conductivity type (n-type in this example) from the trench 20 into the body portion 60, through at least a side wall 22 of a lower part 20b of the trench 20, so as to form the first region 61.

A specific embodiment will now be described, in which the body portion 60 is a low-doped p-type epitaxial layer grown on the highly-doped n-type substrate region 14. This layer may have a uniform doping concentration N_a . Alternatively, its doping concentration N_a may, for example, increase towards the top surface 10a, if such an increasing doping concentration N_a is desired for the regions 62. The channel-accommodating region 15 is a separately-doped region formed in this epitaxial layer by, for example, implantation of boron ions. The boron implantation into the epitaxial layer may be carried out either before or after etching and/or filling the trench 20.

Figure 3 illustrates the situation in which the trench 20 is etched into the epitaxial layer after providing the region 15. The trench etchant mask 40 may still be present on the body during the outdiffusion of the regions 61. A doped material 70 is then deposited and etched back until the doped material 70 is left in only the lower part 20b of the trench 20. The doped material 70 may be the finally desired dielectric material 17, except that it also contains a donor dopant such as arsenic or phosphorus at this stage in the manufacture.

The semiconductor body is now heated to out-diffuse the donor dopant from material 70 to form the first region 61. The resulting first region 61 adjacent to the side wall 22 of the lower part 20b of the trench 20 has a doping concentration N_d of the first conductivity type that is higher than the doping concentration N_a of the second conductivity type of the body portion 60. Its diffusion depth W_1 (measured perpendicular to said side wall 22) is less than the remaining width W_2 of the body portion 60 (also measured perpendicular to said side wall 22).

When a different dielectric material is desired in the lower part 20b of the trench, the material 70 is now etched from the trench 20 and replaced with the different material 17. The trench-gate 11 is then provided in the upper part 20a of the trench 20. Usually the capacitive coupling of the gate 11 to the channel-accommodating region 15 is via a gate insulating layer 24. In this case, a thermal oxidation process may be carried out in known manner to form the insulating layer 24 as silicon dioxide at the side walls 21 of the upper part 20a of the trench 20. When the dielectric material 17 is of undoped or low-doped silicon, then the silicon dioxide layer 24 formed by oxidation extends additionally at the upper face of the dielectric material 17. Conductively doped polycrystalline silicon is then deposited to provide the gate 11. This polycrystalline silicon is generally n-type for the present example of an N-channel device. Its upper surface is oxidised to form an insulating overlayer 23.

The n-type source region 13 is typically a dopant implanted surface region of arsenic or phosphorus in the semiconductor body 1. It may be formed after providing the trench-gate 11, or it may be a remaining part of an

n-type layer formed at the body surface 10a before etching the trench 20. In yet another form when the gate 11 and overlayer 23 form a step at the top surface 10a, the source region 13 may be an n-type shoulder portion formed in a manner similar to that described in United States patent specification
5 US-A-5,378,655 (our ref: PHB33836), by etching back an n-type silicon layer deposited over this step.

The source and drain electrodes 33 and 34 are now provided, typically comprising aluminium. The source electrode 33 normally contacts the region 15, as well as the source region 13. For this purpose a window may be etched
10 in the source region 13 before depositing the source electrode 33.

No plan view of the cellular layout geometry is shown in the drawings, because the invention may be used with quite different, known cell geometries. Thus, for example the cells 1 may have a square geometry as illustrated in Figure 14 of US-A-5,378,655, or they may have a close-packed hexagonal
15 geometry or an elongate stripe geometry. The trench 20 (with its gate 11) may extend around the boundary of each cell 1. Figure 1 shows only a few cells 1, but typically the device comprises many thousands of these parallel cells 1 between the electrodes 33 and 34. The active cellular area of the device may be bounded around the periphery of the body 10 by various known peripheral
20 termination schemes (also not shown). Such schemes normally include the formation of a thick field-oxide layer at the peripheral area of the body surface 10a, before the transistor cell fabrication steps. Furthermore, various known circuits (such as gate-control circuits) may be integrated with the device in an area of the body 10, between the active cellular area and the peripheral
25 termination scheme. Typically their circuit elements may be fabricated with their own layout in this circuit area using some of the same masking and doping steps as are used for the transistor cells 1.

In a specific example of this embodiment of Figures 1 and 2, the doping concentrations of the various regions may be as follows:

- 30
- of the order of 10^{15} cm^{-3} for Na of the second region 62;
 - of the order of 10^{16} cm^{-3} for Nd of the first region 61;

- 10^{16} to 10^{17} cm^{-3} boron doping for the channel-accommodating region 15;
- an additional surface doping of 10^{18} to 10^{19} boron atoms cm^{-3} where the region 15 is contacted by the source electrode 33, and
- 5 • 10^{20} to 10^{22} cm^{-3} for phosphorus or arsenic doping of the source and drain regions 13 and 14.

As regards the doping content of the regions 61 and 62, a sufficient charge balance to avoid avalanche breakdown is required for the depleted regions 61 and 62. The critical field strength for monocrystalline silicon material is approximately 3×10^5 volts. cm^{-1} , and this corresponds to a fully depleted dopant dose of at most approximately 1×10^{12} cm^{-2} . Thus, for the region 62 which is depleted from opposite sides by the two adjacent regions 61 of neighbouring trenches 20, the product ($\text{Na} \cdot \text{W2}$) of the doping concentration Na and width W2 should be at most approximately 2×10^{12} cm^{-2} , whereas for the region 61 adjacent to insulating material 17 in the trench 20, the product ($\text{Nd} \cdot \text{W1}$) of the doping concentration Nd and width W1 should be at most approximately 1×10^{12} cm^{-2} .

Figure 4 shows the results of numerical device simulations of the breakdown voltage V_B in volts and on-resistance R_{on} in $\text{ohm} \cdot \text{mm}^2$, for a conventional trench-gate device and for a specific example of the trench-gate device of Figures 1 and 2 in accordance with the invention. Both devices have a stripe cell geometry. The point A in Figure 4 is for the device of Figures 1 and 2, in which:

- L6 is $41 \mu\text{m}$ for region 61, adjacent an insulating region 17;
- 25 Nd is 1.65×10^{16} , and W1 is $0.5 \mu\text{m}$ for region 61;
- Na is 2×10^{15} , and W2 is $9 \mu\text{m}$ for region 62; and
- the trench-gate 11 is $4 \mu\text{m}$ deep from the surface 10a, with the depth L5 of region 15 being $1.5 \mu\text{m}$; and with L3 of $2 \mu\text{m}$ for part 63 of region 62, between the regions 15 and 61.

30 The breakdown voltage of this device in accordance with the invention is 760 volts with an on-resistance of $4.5 \text{ ohms} \cdot \text{mm}^2$.

The point B is for a conventional device, in which the body portion 16 has a similar length to $(L3+L6)$ but is composed of a single n-type epitaxial layer region having a doping concentration of $1.95 \times 10^{14} \text{ cm}^{-3}$. In this case, the trench-gate 11 is of the same depth as for the Figure 1 device, but the trench 20' does not extend deeper into the body, i.e. the trench 20' does not extend through the depth of the body portion 16. The breakdown voltage of this conventional device is 710 volts with an on-resistance of about 15 ohms.mm².

The curve C shows the theoretical limit for a conventional device having its body portion 16 composed of a single high-resistivity region.

As stated above, a device in accordance with the present invention may have its n-type region 61 adjacent to a low-doped silicon region 17 in the lower part 20b of the trench 20. In this case, the region 61 is depleted from opposite sides by the two adjacent p-type regions 17 and 62, and so its doping concentration Nd can be slightly higher. Thus, the product $(Nd \cdot W1)$ of its doping concentration Nd and width W1 can be at most approximately $2 \times 10^{12} \text{ cm}^{-2}$.

Many other modifications and variations are possible within the scope of the present invention. One such modification is illustrated in Figure 5, in which the upper part 20a of the trench 20 is wider than the lower part 20b. This trench structure can be formed in a modification of the method illustrated in Figure 3. In this modification, the doped material 70 may occupy both the lower and upper parts of the trench 20 during the out-diffusion of the n-type dopant Nd. In this case, the diffused first region 61 is formed not only adjacent to the lower sidewall 22, but also adjacent to the upper sidewall of the trench. The upper part of the trench is then widened by further etching, for example through the etchant mask 40, so as to remove the Nd doping from the sidewall of the now-widened upper part 20a of the trench. The gate 11 is subsequently provided in this widened upper part 20a, in the same manner as earlier described.

Figure 6 illustrates a further variant, that is a modification in accordance with the present invention of the process and trench-gate structure described in the United States patent specification US-A-4,914,058. The whole contents

of US-A-4,914,058 are hereby incorporated herein as reference material. In the Figure 6 device, both the gate 11 and the gate insulating layer 24 extend into the lower part 20b of the trench 20. The lower part 11b of the gate 11 acts as a field plate extension of the gate. The insulating layer part 24b in the lower trench part 20b is thicker than the gate insulating layer 24 in the upper trench part 20a. Thus, the capacitive coupling between the gate 11 and the first region 61 of the body portion 16 is reduced by this greater thickness of the insulating layer part 24b. In the manufacture of the device of Figure 6, the upper and lower parts 20a and 20b of the trench 20 can be formed using process steps as described in US-A-4,914,058. The upper trench part 20a can be first formed by etching, and then a gate insulating layer 24 of silicon dioxide and a lining of, for example, silicon nitride can be formed on the sidewalls of the trench part 20a. Subsequently, the lower trench part 20b can be formed by etching via the exposed bottom of the upper trench part 20a, as described in US-A-4,914,058. Dopant material of the first conductivity type (n-type) is then deposited, and the first region 61 is formed by dopant outdiffusion from the lower trench part 20b. The side walls of the upper trench part 20a are masked against the dopant by the gate insulating layer 24 of silicon dioxide and the lining of silicon nitride. The thicker insulating layer part 24b is formed by, for example, oxidation of the lower trench part 20b. The gate material is then deposited on the insulating layer 24 in the whole trench 20 (both parts 20a and 20b).

An n-channel device has been described with reference to Figures 1 to 6. However, a p-channel device is also possible in accordance with the invention, in which the regions 13, 14 and 61 are p-type, the regions 15 and 62 are n-type, and the conduction channel 12 is of holes.

A vertical discrete device has been described with reference to Figures 1 to 6, having its drain electrode 34 contacting the drain region 14 at the back surface 10b of the body 10. However, an integrated device is also possible in accordance with the invention. In this case, the drain region 14 may be a doped buried layer between a device substrate and the epitaxial body region 60 (62) and may be contacted by electrode 34 at the front major surface 10a

via a doped peripheral contact region which extends from the surface 10a to the depth of the buried layer.

The device illustrated in the drawings is a MOSFET in which the drain region 14 is connected ohmically to a drain electrode 34. The present invention may also be applied to IGBTs (insulated-gate bipolar transistors) of the trench-gate type, in which an emitter region of the opposite conductivity type is present between the drain region 14 and the corresponding main electrode 34 (usually called a "collector" electrode or "anode" electrode of the IGBT). This emitter region forms a p-n junction with a lower doped region 14 to modulate the conductivity of the regions 14 and 16 by carrier injection in the on-state of the IGBT.

From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications may involve equivalent and other features which are already known in the design, manufacture and use of semiconductor devices, and which may be used instead of or in addition to features already described herein. Although Claims have been formulated in this Application to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any Claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The Applicants hereby give notice that new Claims may be formulated to any such features and/or combinations of such features during the prosecution of the present Application or of any further Application derived therefrom.

CLAIMS

1. A trench-gate semiconductor device comprising a semiconductor body including a channel-accommodating region of a second conductivity type between source and drain regions of an opposite first conductivity type, the source region being adjacent to a major surface of the body, from which a trench extends through the channel-accommodating region and into an underlying body portion between the channel-accommodating region and the drain region, a gate being present in an upper part of the trench and capacitively coupled to the channel-accommodating region adjacent to a side wall of the upper part of the trench, and the body portion being present adjacent to the lower part of the trench and comprising first regions of the first conductivity type interposed with second regions of the second conductivity type to carry a depletion layer from the drain region to the channel-accommodating region in an off state of the device and to provide parallel current paths along the first regions in a conducting state of the device, characterised in that the first region is present between the second region and the side wall of the lower part of the trench, is carried through the body portion to the drain region by the lower part of the trench, has a width measured perpendicular to said side wall that is less than the width of the second region, and has a doping concentration of the first conductivity type that is higher than the doping concentration of the second conductivity type of the second region.

2. A device as claimed in Claim 1, further characterised in that the first region adjacent to the lower part of the trench is spaced from the channel-accommodating region by a part of the second region that extends adjacent to the upper part of the trench where the gate is present.

3. A device as claimed in Claim 1 or Claim 2, further characterised in that the first region has a doping concentration of the order of 10^{16} cm^{-3} , and the second region has a doping concentration of the order of 10^{15} cm^{-3} .

4. A device as claimed in any one of the preceding Claims, further characterised in that the upper part of the trench is wider than the lower part of the trench.

5 5. A device as claimed in any one of the preceding Claims, further characterised in that the lower part of the trench is filled with insulating material.

6. A device as claimed in any one of Claims 1 to 4, further
10 characterised in that the lower part of the trench comprises a semiconductor region of the second conductivity type that forms a p-n junction with the first region.

7. A device as claimed in any one of Claims 1 to 4, further
15 characterised in that the gate is capacitively coupled to the channel-accommodating region via a gate insulating layer at the side wall of the trench, in that both the gate and the gate insulating layer extend into the lower part of the trench, and in that the gate insulating layer is thicker in the lower part of the trench than in the upper part so as to reduce the capacitive
20 coupling between the gate and the first region of the body portion.

8. A device as claimed in any one of the preceding Claims, further characterised in that, in the depth direction of the trench, the first region has a length adjacent to the lower part of the trench that is longer (for example an
25 order of magnitude longer) than that of the channel-accommodating region adjacent to the upper part of the trench.

9. A method of manufacturing a trench-gate semiconductor device as claimed in any one of the preceding Claims, wherein the first region has a
30 doping concentration which corresponds to a dopant diffusion profile from the lower part of the trench and which is formed by process steps in which the trench is etched into a body portion of the second conductivity type having a

doping concentration for providing the second region, and dopant of the first conductivity type is out-diffused from the trench into the body portion, through at least a side wall of a lower part of the trench, so as to form the first region adjacent to the side wall of the lower part of the trench with a doping
5 concentration of the first conductivity type that is higher than the doping concentration of the second conductivity type of the body portion and with a diffusion depth measured perpendicular to said side wall that is less than the remaining width of the body portion measured perpendicular to said side wall.

- 10 10. A method as claimed in Claim 9, wherein the body portion of the second conductivity type is provided on the drain region as an epitaxial layer having a uniform doping concentration of the second conductivity type.

[illegible]

FIG. 2

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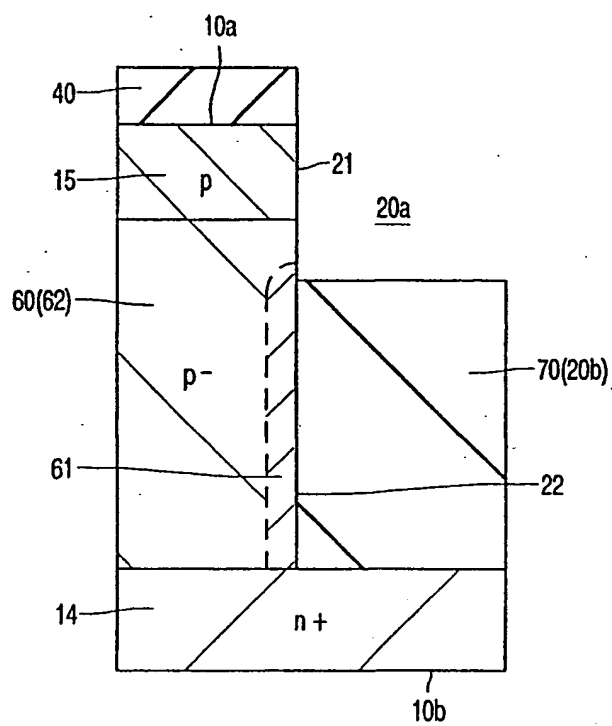


FIG. 3

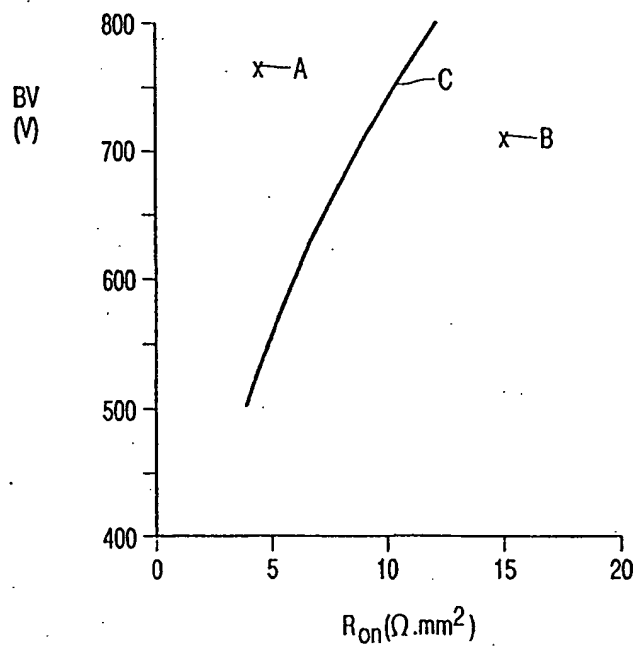
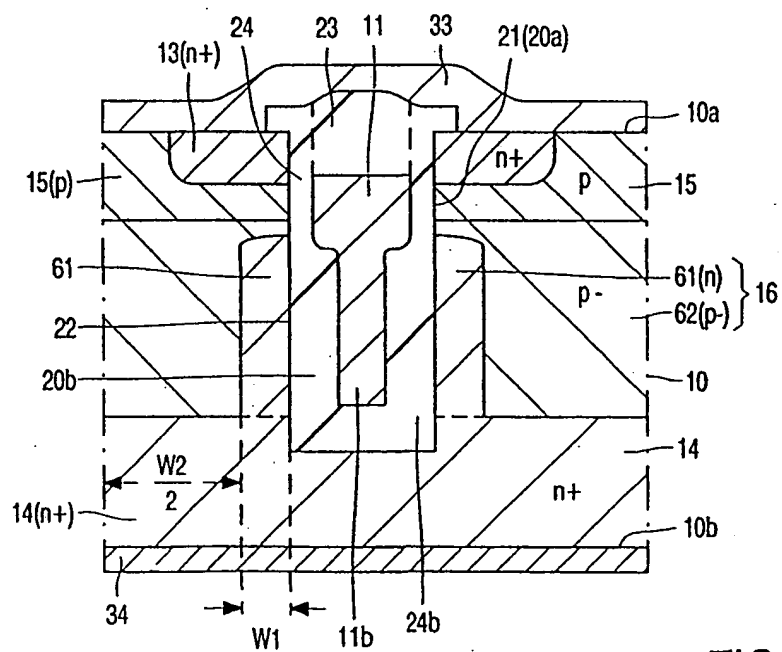
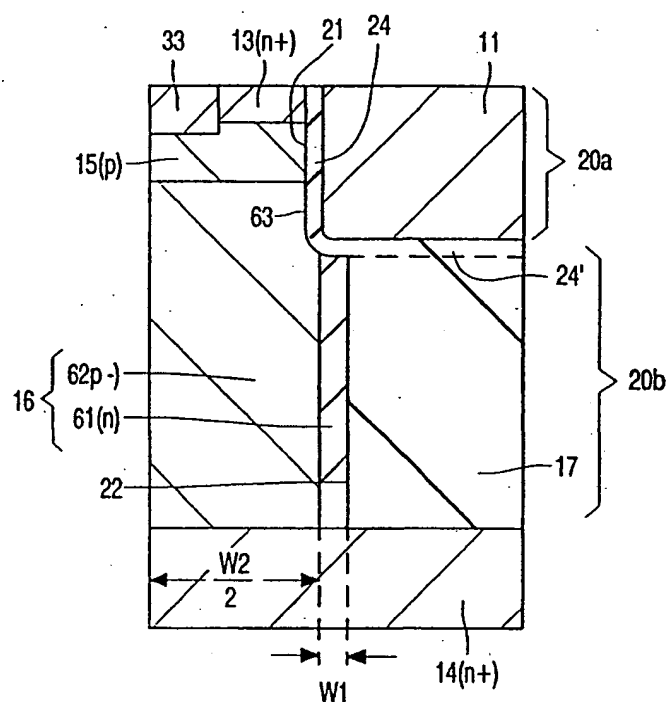


FIG. 4

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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<p>(21) International Application Number: PCT/EP99/08951</p> <p>(22) International Filing Date: 16 November 1999 (16.11.99)</p> <p>(30) Priority Data: 9826041.7 28 November 1998 (28.11.98) GB</p> <p>(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).</p> <p>(72) Inventors: HURKX, Godefridus, A., M.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). HUETING, Raymond, J., E.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).</p> <p>(74) Agent: STEVENS, Brian, T.; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).</p>	<p>(81) Designated States: JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).</p> <p>Published <i>With international search report.</i></p> <p>(88) Date of publication of the international search report: 16 November 2000 (16.11.00)</p>	
<p>(54) Title: TRENCH-GATE SEMICONDUCTOR DEVICES AND THEIR MANUFACTURE</p>		
<p>(57) Abstract</p> <p>In a trench-gate semiconductor device, for example a cellular power MOSFET, the gate (11) is present in a trench (20) that extends through the channel-accommodating region (15) of the device. An underlying body portion (16) that carries a high voltage in an off state of the device is present adjacent to a side wall of a lower part (20b) of the trench (20). Instead of being a single high-resistivity region, this body portion (16) comprises first regions (61) of a first conductivity type interposed with second regions (62) of the opposite second conductivity type. In the conducting state of the device, the first regions (61) provide parallel current paths through the thick body portion (16), from the conduction channel (12) in the channel-accommodating region (15). In an off-state of the device, the body portion (16) carries a depletion layer (50). The first region (61) of this body portion (16) is present between the second region (62) and the side wall (22) of the lower part (20b) of the trench (20) and has a doping concentration (Nd) of the first conductivity type that is higher than the doping concentration (Na) of the second conductivity type of the second region (62). A balanced space charge is nonetheless obtained by depletion of the first and second regions (61, 62), because the width (W1) of the first region (61) is made smaller than the width (W2) of the lower-doped second region (62). This device structure can have a low on-resistance and high breakdown voltage, while also permitting its commercial manufacture using dopant out-diffusion from the lower trench part (20b) into the lower-doped second region (62) to form the first region (61).</p>		

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INTERNATIONAL SEARCH REPORT

International Application No

PCT/EP 99/08951

A. CLASSIFICATION OF SUBJECT MATTER

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

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Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	DE 197 02 102 A (FUJI ELECTRIC CO LTD) 24 July 1997 (1997-07-24) column 25, line 46 - line 51; figure 12	1
A	US 5 216 275 A (CHEN XINGBI) 1 June 1993 (1993-06-01) figure 4	1,3,6,9
	-/-	

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Date of the actual completion of the international search

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A	<p>PATENT ABSTRACTS OF JAPAN vol. 018, no. 225 (E-1541), 22 April 1994 (1994-04-22) -& JP 06 021468 A (TOSHIBA CORP), 28 January 1994 (1994-01-28) abstract; figures 1-4</p>	9,10

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Information on patent family members

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